IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/562,293
Applicant	:	Peter W. GREEN
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Examiner	:	Nicholas J. Tobergte
Atty. Docket	:	GB-020136US

Title: THIN FILM TRANSISTOR

APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Window, Mail Stop **Appeal Brief - Patents**
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

In response to the FINAL Office Action dated 10 July 2007 and the Advisory Action dated 29 October 2007, finally rejecting pending claims 24-28, and in support of the Notice of Appeal filed on 27 November 2007, Applicant hereby respectfully submits this Appeal Brief.

REAL PARTY IN INTEREST

According to an assignment recorded at Reel 017416, Frame 0911, Koninklijke Philips Electronics N.V., owns all of the rights in the above-identified U.S. patent application.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences related to this application or to any related application, nor will the disposition of this case affect, or be affected by, any

other application directly or indirectly.

STATUS OF CLAIMS

Claims 1-23 are cancelled and claims 24-28 are pending and all stand rejected.

Accordingly, the claims on Appeal are claims 24-28.

STATUS OF AMENDMENTS

There are no pending amendments with respect to this application.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a thin film transistor (TFT), which, for example, may be used in an active matrix liquid crystal display.[1]

Accordingly, as broadly recited in claim 24, a thin film transistor (TFT) (FIGs. 2, 3I, 4 and 6) comprises: a gate (element 4 - FIGs. 2, 3I, 4 and 6; page 5, line 5) disposed on a substrate (element 1 - FIGs. 2, 3I and 6; page 5, lines 5-6), the gate having side edges (elements 4a & 4b - FIG. 3B – page 6, lines 9-10) inclined towards one another to reach a tip (element 13 – FIG. 3B – page 6, line 10; page 7, lines 6-7; page 8, lines 3-4) having a radius of a few nanometers (page 6, line 11); a gate insulating layer (element 5 - FIGs. 2, 3I, 4 and 6 – page 5, lines 7-8) disposed on the gate; a channel region (element 6 - FIGs. 2, 3I, 4 and 6 – page 7, lines 11-12) disposed on the gate insulating layer; a source electrode (element 8a - FIGs. 2, 3I, 4 and 6 – page 7, lines 21-22) overlying a first side edge of the gate, and a drain electrode (element 8b - FIGs. 2, 3I, 4 and 6 – page 7, lines 21-22) overlying a second side edge of the gate.

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1 In the description to follow, citations to various reference numerals, figures, and corresponding text in the specification are provided solely to comply with Patent Office rules. It should be understood that these reference numerals, figures, and text are exemplary in nature, and not in any way limiting of the true scope of the claims. It would therefore be improper to import anything into any of the claims simply on the basis of **exemplary** language that is provided here only under the obligation to satisfy Patent Office rules for maintaining an Appeal.

As broadly recited in claim 25, the TFT further features a layer of doped semiconductor material (element 7 - FIGs. 2, 3I, 4 and 6 – page 5, lines 10-11) overlying the channel region.

As broadly recited in claim 26, the TFT further features the channel region having a length ("L" in FIG. 2) of 20-40 nanometers (page 5, line 12).

As broadly recited in claim 27, the TFT further features an insulating material (element 16 – FIG. 6; page 8, lines 14-21) disposed between the gate and the substrate.

As broadly recited in claim 28, the TFT further features the channel region comprising intrinsic amorphous silicon (page 6, line 11).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on Appeal are: (1) the rejections of claims 24, 25, 27 and 28 under 35 U.S.C. § 102 over Yamazaki et al. U.S. Patent 6,501,094 ("Yamazaki"); and (2) the rejection of `claim 26 under 35 U.S.C. § 102 over Yamazaki.

ARGUMENTS

(1) Claims 24-25 and 27-28 Are All Patentable Over Yamazaki

Claim 24

Among other things, the TFT of claim 24 includes a gate disposed on a substrate, the gate having side edges inclined towards one another to reach a tip having a radius of a few nanometers.

At the outset, the Examiner states that a tip can be flat or rounded.

Applicant respectfully disagrees.

At the outset, the American Heritage Dictionary, for example, defines "tip" as *"the end of a pointed or projecting object."* This definition is entirely consistent with the clear meaning of "tip" as defined by usage in the specification of this patent application.

On the other hand, an "interpretation" of "tip" as meaning "flat or rounded" is totally inconsistent with the term as defined in the specification (see, e.g., FIGs. 2-4

and 6 and the accompanying text at page 5, lines 13-14; page 6, lines 9-11 as contrasted with the "*flat top region 15*" of FIG. 5 described at page 8, line 1).

The Examiner states that Applicant's specification discloses that a tip "can be blunted."

So what? Of course a tip can be blunted . . . and after it is blunted, then it is no longer a tip! That is like saying that a bubble can be burst. Again, of course a bubble can be burst . . . but once that is done, it is no longer a bubble!

Here, the claim clearly recites that the TFT includes a gate ***having*** side edges inclined towards one another to reach a tip . . . not a gate that "had" side edges inclined towards one another to reach a tip that was then blunted.

Yamazaki does not disclose any TFT that EVER has side edges inclined towards one another to reach a tip.

So Yamazaki does not disclose the TFT of claim 24.

Furthermore, Applicant respectfully submits that Yamazaki does not disclose any gate having side edges inclined towards one another to reach ***a tip having a radius of a few nanometers***. As explained in the specification, by providing the device with a real tip having a very small radius (in contrast to Yamazaki which has a flat, plateau-like top that the Examiner calls a "tip") provides a device with short channel length, reduced stray capacitance, and an increased aspect ratio for a display device incorporating the TFT. See, e.g., page 1, lines 18-19; page 2, lines 28-29; page 3, lines 9-14; and page 8, lines 11-13.

The Examiner states that Yamazaki does disclose a gate having side edges inclined towards one another to reach a tip having a radius of a few nanometers.

However, the Examiner fails to cite anything at all in Yamazaki that actually discloses any tip ***having a radius of a few nanometers***.

In response to this, in the Advisory Action dated 29 October 2007, the Examiner states that such a feature is inherent in Yamazaki.

Applicant respectfully disagrees.

M.P.E.P. § 2112(IV) provides that:

> The fact that a certain result or characteristic may occur or be present

> in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); In re Oelrich, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "*To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is* ***necessarily present*** *in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however,* ***may not be established by probabilities or possibilities****. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.*' " In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted) . . . "*In relying upon the theory of inherency, the examiner* ***must*** *provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic* ***necessarily*** *flows from the teachings of the applied prior art*." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990).

(Emphasis Added)

Here, the Examiner has clearly failed to meet this burden. The Examiner states that "*TFTs are measured in are* (sic) *on the nanometer scale*."

Well, to be specific, with respect to FIG. 1A Yamazaki discloses that the thickness of titanium film pattern 102 is a few (e.g., 20) nanometers (Yamazaki at col. 5, lines 55-56). It is also quite apparent from inspection of FIG. 1A that the width of the flat plateau region at the top of the gate formed by films 102 and 103 is several times the thickness of titanium film pattern 20. So, at most, Yamazaki suggests that the flat plateau at the top of its gate is maybe 200-300 nanometers. This can hardly be categorized under any definition as "a few" nanometers.

The Examiner states that the quantity "a few" is not defined. The Examiner has not contended that this is indefinite. So it should be defined as one of ordinary

skill in the art would understand it, in light of the specification. Applicant respectfully submits that no reasonable person would ever define "a few" to include "200-300."

Meanwhile, the manufacturing process and device disclosed by Yamazaki do not even remotely suggest any modifications that would produce such a small, true tip of a few nanometers at most, and so this feature could not be obtained by any simple change or "optimization" of process parameters in Yamazaki.

Accordingly, for at least this reasons, claim 24 is deemed patentable over Yamazaki.

Claim 25

Claim 25 depends from claim 24 and is deemed patentable for at least the reasons set forth above with respect to claim 24.

Claim 27

Claim 27 depends from claim 24 and is deemed patentable for at least the reasons set forth above with respect to claim 24, and for the following additional reasons.

Among other things, the TFT of channel 27 includes an insulating material disposed between the gate and the substrate.

The Examiner cites insulating material 407 in FIG. 4C of Yamazaki.

However, insulating material 407 in FIG. 4C of Yamazaki is not disposed between the gate and the substrate. The substrate in FIG. 4C of Yamazaki corresponds to the region labeled 401 in FIG. 4A on the same page. The gate in FIG. 4C of Yamazaki corresponds to the two regions labeled 402 and 404 in FIG. 4A on the same page (see also col. 9, lines 54-56 "*a gate electrode comprised of a titanium film pattern 402 and an aluminum film pattern 404 is formed on a glass substrate 401*"). It is apparent from FIGs. 4A-C that ***the gate electrode 402/404 is in direct contact with substrate 401 without anything (and specifically without insulating material 407) being disposed therebetween***.

Accordingly, for at least these additional reasons, Applicant respectfully submits that claim 27 is patentable over Yamazaki.

Claim 28

Claim 28 depends from claim 24 and is deemed patentable for at least the

reasons set forth above with respect to claim 24.

(2) Claim 26 is Patentable Over Yamazaki

Claim 26 depends from claim 24 and is deemed patentable for at least the reasons set forth above with respect to claim 24, and for the following additional reasons.

Among other things, in the TFT of channel 26 the channel region has a length of 20-40 nanometers.

Yamazaki does not disclose a TFT having so small of a channel region, nor is Yamazaki suitable for providing such a small channel region because Yamazaki teaches a gate having a flat, plateau-like top having a width of 200-300 nanometers that necessary produces a channel length much greater than 20-40 nanometers, such as can be produced by a gate having a tip having a radius of a few nanometers, as in the TFT of claim 26. No amount of experimentation with Yamazaki with its gate having a flat, plateau-like top would ever produce a device with such a small channel region. So, in re Aller, Lacey and Hall, 220 F.2d 454, 105 USPQ 233 (CCPA 1955) cited by the Examiner, is inapplicable to the extent that it even stands for the proposition stated by the Examiner (see Eibel Process Co. v. Minnesota & Ontario Paper Co., 261 U.S. 45, 68 (1923)).

The Examiner also incorrectly states that the specification does not teach the critical nature of the small channel width of claim 26 – a smaller channel length than anything disclosed by Yamazaki. See, e.g., page 1, lines 18-19; page 2, lines 28-29; page 3, lines 9-14; and page 8, lines 11-13 of the present specification which clearly discloses the substantial benefits that can only be provided with a device having such a small channel width.

Accordingly, for at least these additional reasons, Applicant respectfully submits that claim 26 is patentable over Yamazaki.

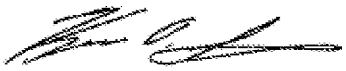
CONCLUSION

For all of the foregoing reasons, Applicant submits that claims 24-28 are all patentable over the cited prior art. Therefore, Applicant respectfully requests that the

rejections of claims 24-28 be withdrawn, the claims be allowed, and the application be passed to issue.

Respectfully submitted,

VOLENTINE & WHITT



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CLAIMS APPENDIX

1-23. (Canceled).

24. (Previously Presented) A thin film transistor (TFT), comprising:

a gate disposed on a substrate, the gate having side edges inclined towards one another to reach a tip having a radius of a few nanometers,

a gate insulating layer disposed on the gate;

a channel region disposed on the gate insulating layer;

a source electrode overlying a first side edge of the gate, and

a drain electrode overlying a second side edge of the gate.

25. (Previously Presented) The TFT of claim 24, further comprising a layer of doped semiconductor material overlying the channel region.

26. (Previously Presented) The TFT of claim 24, wherein the channel region has a length of 20-40 nanometers.

27. (Previously Presented) The TFT of claim 24, further comprising an insulating material disposed between the gate and the substrate.

28. (Previously Presented) The TFT of claim 24, wherein the channel region comprises intrinsic amorphous silicon.

EVIDENCE APPENDIX

American Heritage Dictionary, Fourth Edition, 2000

RELATED PROCEEEDINGS APPENDIX

{None}